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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,338	03/26/2001	Futoshi Kawarazaki	034620-088	6335

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,338	KAWARAZAKI, FUTOSHI	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/27/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 March 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-9 are presented for examination.

Election/Restrictions

Claim 9 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on May 27, 2004.

Applicant's arguments, in the reply filed on May 27, 2004, with respect to the requirement for election/restriction have been fully considered and are persuasive. The restriction requirement made in the Office action mailed on March 24, 2004 is hereby withdrawn.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received with papers filed on March 6, 2001.

Drawings

The drawings were received on March 26, 2001. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Inagaki U.S. Patent No. 6,421,773.

As per claim 1, Inagaki teaches a sequence control circuit with and instruction memory. This sequence control circuit has, in addition to the above sequence control instruction area, an address operation area, a data operation area and a control, signal generation instruction area provided in a memory area of each address of instruction memory. The address operation area, the data operation area, and the control signal generation instruction area are provided in the operand storing area. When the instruction memory is accessed by the address outputted from the program counter, instructions for address generation, test data generation and control signal generation are read from the address operation area, the data operation area and the control signal generation instruction area and then supplied to the address generator, the test data generator and the control signal generator, respectively. The program counter

controller receives an operation code part of sequence control instructions from the instruction memory, a match flag MFLG from the logic comparator and an output of the index counter. Based on the result obtained by decoding the instruction stored in the instruction memory, on the match flag MFLG, and on an output from the index counter, the program counter controller controls the program counter and the stack register. In the concrete, the program counter controller handles a content of the program counter, that is, the value showing an address to be read next in the instruction memory, through increment (n+1), decrement or hold operation, and loads the value to the program counter. (Figures 1 and 2, column 2 lines 20-52 column 7 lines 11-293)

As per claims 2 and 3, Inagaki teaches a sequence control circuit provided in a test pattern generator of a memory test apparatus for performing a test of a semiconductor memory device. The sequence control circuit has an instruction memory for storing each of the instructions of the test program, a plurality of branch address registers each for storing a branch address, a logic operation circuit for receiving a plurality of flags and detecting a combination of flag values, a program counter for outputting an address to the instruction memory, a program counter controller for controlling the program counter according to a control word read from the instruction memory and selecting one of the branch address registers corresponding to a combination of the flag values, in which the branch address stored in the branch address register selected by the program counter controller is loaded in the program counter. The sequence control circuit, according to the detection result of a combination of a number of flags which represent branch conditions, the address to be

loaded into the program counter is switched. When a time-out occurs during block erasing operation in a flash memory test, the flash memory has been considered defective as it is in the test according to the conventional test pattern. However, in this case, the memory is good and usable in the blocks other than the block showing the time-out. Therefore, it is only necessary to jump to any other block to continue the test without merely discarding the useful memory as defective. (Column 4 lines 1-32, column 6 lines 45-67, Figure 3)

As per claim 4, Inagaki teaches the instruction memory has a pair of sequence control instruction areas for storing an operation code part and an operand storing area for storing an operand. (Column 5 lines 12-17, Figures 2, 3)

As per claim 5, Inagaki teaches a plurality of branch address registers. (Column 5 lines 48-57, Figures 2, and 3)

As per claim 6, Inagaki teaches a sequence control circuit test has an instruction memory for storing each of the instructions of the test program, a plurality of branch address registers each for storing a branch address, a logic operation circuit for receiving a plurality of flags and detecting a combination of flag values, a program counter for outputting an address to the instruction memory, a program counter controller for controlling the program counter according to a control word read from the instruction memory and selecting one of the branch address registers corresponding to a combination of the flag values, in which the branch address stored in the branch address register selected by the program counter controller is loaded in the program counter. (Column 4 lines 1-32, column 6 lines 45-67, Figure 3)

As per claim 7, Inagaki teaches a program counter controller that receives an operation code part of sequence control instructions from the instruction memory, an output from the logic operation circuit and an output of the index counter. The program counter controller controls the program counter and the stack register based on the result obtained by decoding the instructions stored in instruction memory and based on the outputs from the logic operation circuit and the index counter. In the concrete, the program counter controller handles a content of the program counter, that is, the value showing an address to be read next in the instruction memory, through the increment, decrement or hold operation and loads the value into the program counter.
For loading the above value to the program counter, the program counter controller arranges according to the instructions read out so that any one of (i) an operand of the instruction for a present address of the instruction memory, (ii) a content of the starting address register, (iii) contents of the branch address registers, and (iv) a content of the stack register is set to the program counter as the value. (Figures 2, 3 and Column 5 lines 18-38)

As per claim 8, Inagaki teaches implementation of a sequence control circuit within a semiconductor testing apparatus. (Column 8 lines 22-38, Abstract)

As per claim 9, Inagaki teaches Inagaki teaches implementation of a sequence control circuit within a semiconductor testing apparatus with and instruction memory. This sequence control circuit has, in addition to the above sequence control instruction area, an address operation area, a data operation area and a control, signal generation instruction area provided in a memory area of each address of instruction memory. The

address operation area, the data operation area, and the control signal generation instruction area are provided in the operand storing area. When the instruction memory is accessed by the address outputted from the program counter, instructions for address generation, test data generation and control signal generation are read from the address operation area, the data operation area and the control signal generation instruction area and then supplied to the address generator, the test data generator and the control signal generator, respectively. The program counter controller receives an operation code part of sequence control instructions from the instruction memory, a match flag MFLG from the logic comparator and an output of the index counter. Based on the result obtained by decoding the instruction stored in the instruction memory, on the match flag MFLG, and on an output from the index counter, the program counter controller controls the program counter and the stack register. In the concrete, the program counter controller handles a content of the program counter, that is, the value showing an address to be read next in the instruction memory, through increment (n+1), decrement or hold operation, and loads the value to the program counter. (Figures 1 and 2, column 2 lines 20-52, Column 8 lines 22-38, Abstract)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,615,218 Tsurumi

This patent teaches a test pattern generation device for testing semi-conductor devices. The device generates high capacity patterns much more quickly than is possible with the conventional test pattern generator while permitting the use of the conventional layout of the test patterns and the common operational features of the existing test pattern generators. The control circuit stores an index address in the address pointer. Upon receiving a transfer command, the index is outputted to the execution memory, and the leading address data thus read out is stored in the modifier register. Next, the address generator is activated, and the address data and the output of the modifier register are added by the adder. The added result is inputted into the execution memory via the selector. This process is repeated successively for other leading address data, and the test patterns are thus outputted from the execution memory without the use of a buffer memory used in the conventional types of test pattern generators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

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